REMARKS

Applicants respectfully traverse and request reconsideration.

Claim Rejections under 35 U.S.C. § 102(b)

Claims 14-17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Leondires et al. U.S. Patent No. 5,841,763 (Leondires).

Leondires is directed to an audio video conferencing system. (Leondires, title). Fig. 3 of Leondires is a block diagram of an MCU (multipoint connection unit) 102 including a host processor 174 and DSP board assemblies 180 through 194. (Leondires, Col. 8, lines 14-41). Each DSP board assembly 180 through 194 is configured as a parent/child combination. (Leondires, Col. 9, lines 42-43). The parent board contains four nodes 180C. (Leondires, Col. 9, lines 43-46). Each node receives instructions from the host 174 regarding which time slots on the HMVIP bus 204 the node is to read information from.

With regards to claim 17, applicants claim, among other things, emulating a specific microprocessor instruction set. Program code is configured to cause a portion of the plurality of processors to emulate a specific microprocessor instruction set. Accordingly, at least one of the plurality of processors emulates a specific microprocessor instruction set. The Applicants' claimed invention, among many advantages, provides the ability and flexibility so that at least one of the plurality of processors may execute a native instruction set as well as emulate a specific microprocessor instruction set. (Specification pages 6-7 and 11-2).

Rather than emulate a specific microprocessor instruction set, Leondires teaches that each node on the DSP board assembly 180 through 194 can execute different code modules downloaded to its respective dual port RAM from the host 174, to accommodate the demands of the teleconferencing system 100. (Leondires, Col. 9, lines 55-50). Therefore, Leondires teaches that each DSP board executes code modules on a corresponding DSP. Since the host downloads the code modules for execution on the DSP, the DSP executes the code modules and therefore does not emulate a specific microprocessor instruction set. As a result, the Leondires reference, as cited, fails to describe each and every element as arranged in claim 17. Consequently, Leondires, as cited in the Office Action, fails to anticipate claim 17. Therefore, for at least the reasons stated above, it is submitted that the present rejection is improper and should be

withdrawn. Reconsideration and passage of the present claims to issuance is respectfully requested.

Dependent Claim 14

Applicants respectfully reassert the arguments made above regarding claim 17. In addition, Applicants also submit that because claim 14 depends from claim 17 and is a dependent claim therefrom, claim 14 is allowable for at least the reasons claim 17 is allowable. Applicants further submit, argued in part at least immediately above, that the dependent claims are also allowable in light of the presence of novel and non-obvious elements contained in claim 14 that are not otherwise present in claim 17.

Claim Rejection under 35 U.S.C. § 103(a)

Claims 2, 3, 5-12, 15 and 16 are rejected under 35 U.S.C. § 103(a) based on Leondires in view of Carmon et al. U.S. Patent No. 4,724,587 (Carmon).

As to Claims 15 and 16, the Office Action acknowledges that Leondires fails to teach queuing tasks as recited in Claims 15 and 16. Carmon is directed to a system for controlling task execution in a host processor based upon the maximum direct memory access (DMA) resources available to a digital signal processor. (Carmon, title). A host processor presents task requests to a signal processor via building a list of packet transfer requests in a partitioned queue in memory. (Carmon, Col. 3, lines 50-54). The host processor accesses the partitioned queue with an interprocessor DMA controller and moves the necessary data signal samples in or out of the signal processor via the DMA mechanism. (Carmon, Col. 3, lines 54-58).

In contrast to Carmon, Leondires teaches that if the host 174 cannot locate any available DSPs, it generates an error and rejects the call from the network. (Leondires, Col. 19, lines 7-9). Therefore, rather than queuing a task for processing when a resource becomes available, Leondires explicitly teaches rejecting the call from the network in direct contradiction to the teachings of queuing packet transfer requests in Carmon. As shown in Fig. 8 of Leondires at step 298, if the host 174 cannot locate any available DSPs, the host generates an error at step 306 and rejects the call from the network 116. (Leondires, Figure 8). Therefore, based on the explicit teachings of Leondires and Carmon, Leondires teaches away from modification by Carmon as suggested in the Office Action. As such, one skilled in the art would not be

motivated to modify Leondires with Carmon as suggested in the Office Action. As a result, the Office Action fails to establish a *prima facie* case of obviousness. Therefore, for at least the reasons stated above, it is submitted that the present rejection is improper and should be withdrawn. Reconsideration and passage of the present claims to issuance is respectfully requested.

With regards to Claim 2, Applicants repeat the above relevant remarks. Among other things, Claim 2 recites that the plurality of processors of the homogenous multiprocessing environment are capable of executing a first instruction of a first instruction set and a second instruction of a second instruction set. As previously stated, Leondires teaches that each node receives instructions from the host 174. (Leondires, Col. 9, lines 59-60). Therefore, rather than teach that the plurality of processors are capable of executing a first instruction set and a second instruction set, Leondires explicitly teaches each node receives instructions from the host 174. Since each node receives the same instructions from host 174, then each node must execute the same instruction set as opposed to a first instruction set and a second instruction set as recited in the claims. As a result, Leondires fails to teach and further teaches away from where each node receives instructions from a first instruction set and instructions from a second instruction set. As a result, Leondires fails to teach "wherein a plurality of processors of the homogeneous multiprocessor environment are capable of executing a first instruction of a first instruction set and a second instruction of a second instruction set." As such, Applicants submit that the present rejection is improper because Leondires fails to teach or suggest all of the claimed limitations as arranged in the claims. Therefore, for at least the reasons stated above, it is submitted that the present rejection is improper and should be withdrawn. Reconsideration and passage of the present claims to issuance is respectfully requested.

With regard to claim 3, Applicants repeat the above relevant remarks, especially those with regard to claim 2 showing that Leondires fails to teach a plurality of processors capable of executing instructions from a first instruction set and from a second instruction set. Further, since Leondires fails to teach where the plurality of processors execute a first instruction set and a second instruction set, Leondires necessarily fails to teach wherein the first instruction and second instruction share an identical bit pattern, but perform different operations. Further, the cited portion of Leondires asserted by the Office Action to teach the identical bit pattern for the

first instruction and the second instruction, merely teaches downloading different software modules to different DSPs at Col. 16, lines 40-41. As such, Applicants submit that the present rejection is improper because Leondires fails to teach or suggest all the claim limitations as arranged in the claims. In addition, Applicants also submit that because dependent claim 3 depends on dependent claim 4 and independent claim 15, as a dependent claim therefrom, claim 3 is allowable for at least the reasons claim 2 is allowable. Applicants further submit, argued in part at least immediately above, that the dependent claims are allowable in light of the presence of novel and non-obvious elements contained in the dependent claims that are not otherwise present in claim 3. Therefore, for at least the reasons stated above, it is submitted that the present rejection is improper and should be withdrawn. Reconsideration and passage of the present claims to issuance is respectfully requested.

Regarding claims 5, 6, 7, 8, 9, 10, 11 and 12, Applicants respectfully reassert the arguments made above, especially those with regards to claims 3 and 15. In addition, Applicants also submit that these claims depend from claim 15 and other intermediate claims and provide further patentable subject matter in view thereof. Further, it is submitted that these claims are allowable not merely as being dependent upon an allowable base claim, but rather contain patentable subject matter in view of the prior art of record. Therefore, reconsideration and withdrawal of the present rejections is respectfully requested.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Leondires in view of Carmon and in further view of Guyer et al. U.S. Patent No. 4,597,041 (Guyer). Applicants respectfully reassert the above relevant remarks, especially those regarding claims 15 and 3 and the remarks showing that Leondires teaches away from modification by Carmon as suggested in the office action. Further, Guyer teaches kernel microcode located in microcode memory rather than wherein a first processor executes an input/output kernel program. Rather than teach an *input/output* kernel program, Guyer merely teaches microcode memory containing only kernel microcode and therefore, Guyer teaches away from an input/output kernel program. Consequently, Guyer fails to teach an input/output kernel program. Since Guyer explicitly teaches away from an input/output kernel program, one would not be motivated to modify the combination of Leondires and Carmon to include an input/output kernel program. As such, Applicants submit that the present rejection is improper because the combination of Leondires,

Carmon and Guyer fail to teach or suggest all of the claim limitations based on the disclosure of Leondires, Carmon and Guyer. Further, since one would not be motivated to modify Leondires with Carmon or with Guyer, the office action fails to establish a *prima facie* case of obviousness. Therefore, for at least the reason stated above, it is submitted the present rejection is improper and should be withdrawn. Reconsideration and passage of the present claims to issuance is respectfully requested.

Accordingly, Applicant respectfully submits that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

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Respectfully submitted,

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